think SPEED think GiDEL™

Product Brief
October 2010

ProcSoC™ SoC/ASIC Verification System

Overview

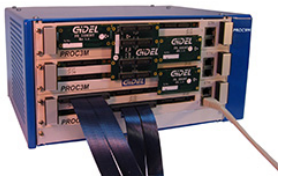
GiDEL's ***ProcSoC*** Verification System provides ***scalability*** of multiple interconnected FPGA modules enabling verification of SoC designs with up to 360 million equivalent ASIC gates. Each ***ProcSoC*** module, itself is a modular and scalable SoC verification system. Fast Gigabit Ethernet connection combined with GiDEL's development tools enable to run the target software or regression suites via remote servers connected to the SoC/ASIC design. The remote operation is performed at near actual system speed allowing for hardware-software integration and co-verification.

The ***ProcSoC*** connects directly to target hardware via high performance I/O's. The application software combined with the system debug tools enable very long DUT runs with visibility to buses and internal nodes. A single ***ProcSoC*** system comprises multiple reconfigurable ***Proc12M***™, ***Proc6M***™ or ***Proc3M***™ boards, each with two interconnected high speed ***Stratix IV 820***, ***Stratix III 340*** or ***Stratix II 180*** FPGAs respectively.

Two chassis configurations are available, ***ProcSoC3*** and ***ProcSoC10***, capable of supporting up to 3 or 10 ***Proc12M/6M/3M*** boards respectively. Each ***ProcSoC*** system can prototype a single SoC device or be partitioned to prototype multiple designs in parallel. The ***ProcSoC***'s unique interconnectivity topology enables any FPGA to connect directly to any other FPGA in the system even in large systems.

Target Applications

- Early hardware/software co-design ("co-verification" at hardware speed)
- Early ASIC/SoC and Intellectual Property (IP) block debug
- Algorithm validation
- Regression tests
- ASIC/SoC integration with target systems
- System integration before committing to silicon
- Prototyping combined with connections to external I/Os



ProcSoC3

ProcSoC10

Key ProcSoC Features

- World's first ASIC Prototyping System
- Scalable up to 360 Million equivalent ASIC gates
- Supported by ***Proc Developer's Kit*** tools enabling advanced, fast and thorough debug methodologies, and real-time co-development
- Flexible direct FPGA interconnectivity for high speed operation and ASIC prototyping
- World's fastest verification system: up to 300MHz
- Multi-user access over the LAN
- Real-time Hardware-Software co-development
- Supported by the PB and PSDB families: application specific daughter boards for enhanced prototyping capabilities
- 1,416 user I/Os per PROCessor board for internal or target system interconnectivity usage
- Up to 2GB of on-board DDR II (512MB/FPGA)
- Additional 2×4GB SODIMMs per selected FPGAs
- 8 global clocks in ProcSoC 3 model

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Find and Resolve More Bugs Faster

The ***ProcSoC*** offers new verification and debug methodologies enabling finding and solving hidden corner-case bugs in highly complex designs.

This task is accomplished by:

Significantly higher execution speed → a large number of test vectors are quickly processed and thus can capture rarely-occurring bugs

ProcWizard™ →

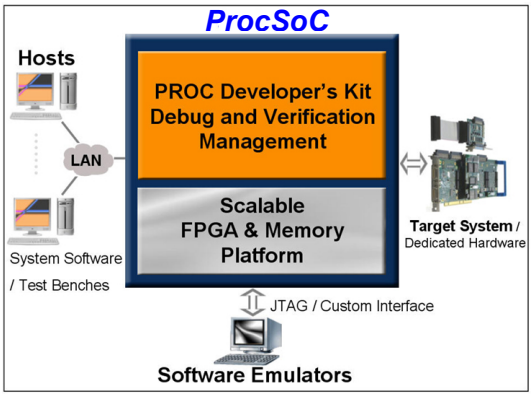
- Host test SW to HW automatic integration
- Host SW/IP automatic integration → simple development of high-level embedded SW

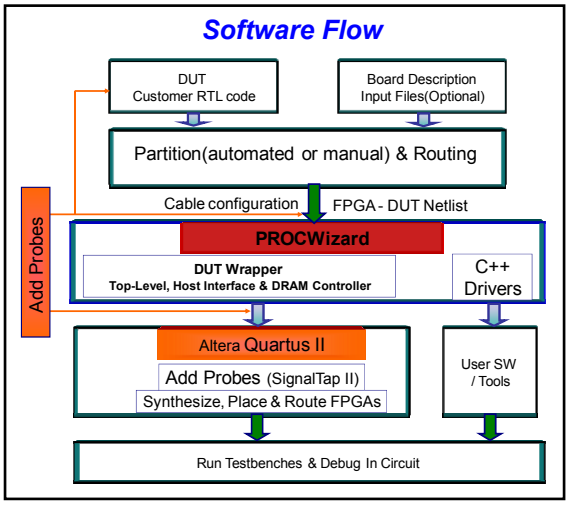
TotalHistory™ → Captures up to 30,000 probe points per FPGA with virtually unlimited depth using on-board memories and enables to view waveform display (VCD format) of trace history

ProcHILs™ → Integration with Simulink™ test environments

SignalTap II → Internal node visibility

Third-party partitioning software → Automatic partitioning
Third-party debug tools software





ProcSoC Model Configurations

Modules	*Proc SoC3-3S (3 boards)*	*Proc SoC10-3S (10 boards)*	*Proc SoC3-4S (3 boards)*	*Proc SoC10-4S (10 boards)*	*3× Proc SoC10-4S (30 boards)*
ASIC Gates	5-15M	10-50M	12-36M	24-120M	132-360M
No. of Stratix III 340	2-6	4-20	—	—	—
No. of Stratix IV 820	—	—	2-6	4-20	22-60
I/O Connections	1,416 – 4,248	2,832 – 14,160	1,416 – 4,248	2,832 – 14,160	15,576-42,480
System Frequency	<=300 MHz	<=300 MHz	<=300 MHz	<=300 MHz	<=300 MHz
FPGA-FPGA LVDS Frequency	1 GHz	1 GHz	1 GHz	1 GHz	1 GHz
FPGA – FPGA Connectivity	<=300 MHz	<=300 MHz	<=300 MHz	<=300MHz	<=300 MHz
On-board DDR II DRAM	256 - 768 MB	512 – 2,560 MB	1 - 3 GB	2 – 10 GB	11 - 30 GB
Total Internal RAM	41-123Mb	82-409.8Mb	50-150Mb	100-500Mb	550Mb-1.5Gb
18*18 Multipliers	1,152 - 3,456	2304-11,520	1920 - 5,760	3,840-19200	21,120-57,600

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