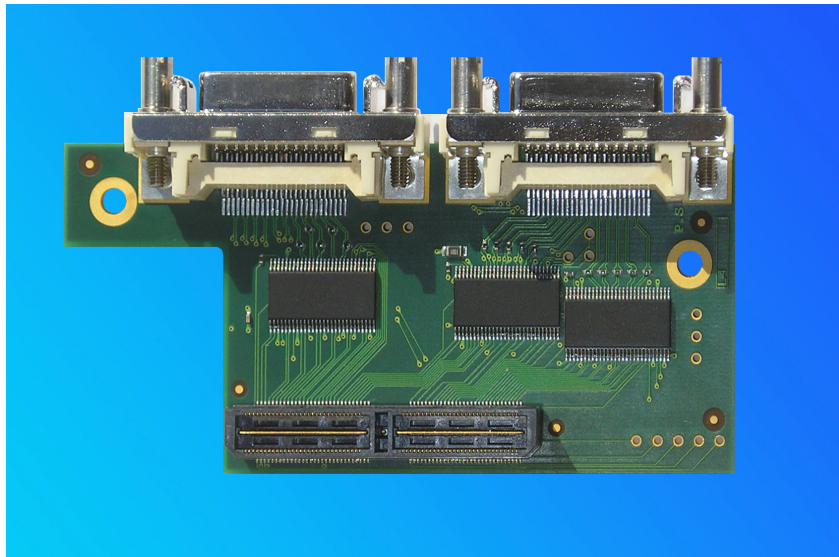


GIDEL **PSDB_CL**

GIDEL PSDB_CL is a type 1 PSDB. This means that uses a single connector to connect to the PROC motherboard. On the PROC boards, this connector is located to the **left** of the target FPGA.

PSDB_CL is designed to provide a CameraLink connection to the PROC motherboard via its panel. Therefore, this daughterboard is intended to be placed on location 1 when possible. Nevertheless, it will work properly when connected to any other location on the PROC board.





GiDEL PSDB_CL™ was designed to provide a simple and convenient way to connect an external camera to **GiDEL PROCStar II™** and **PROCSpark II™** boards.

PSDB_CL key features include:

- ✓ Support of standard CameraLink modes (base, medium, full or dual base assembly)
- ✓ Serial Communication with camera
- ✓ Simple interface
- ✓ Automatic detection by hardware / software
- ✓ Designed to work with **GiDEL PROCCamLink™** IP
- ✓ Automatic integration of PROCCamLink IP into user's top-level design using **GiDEL PROCWizard™**

PSDB_CL uses two MDR 26-pin female connectors (**J1** and **J3**), according the CameraLink standard.

The following adapters are used in PSDB_CL to adapt the CameraLink Signals:

- National Semiconductor **DS90CR288A** for LVDS to LVTTTL adapting of data signals.
- National Semiconductor **DS90LV047A** for LVDS to LVTTTL adapting of control signals.
- National Semiconductor **DS90LV019** for LVDS to LVTTTL adapting of serial control signals.