

# **PROCe III™**

## **PCIe x4 Computation Accelerator**

### Key Features

- Stratix III 80E, 110E, 260E, 150L or 340L FPGAs
- 4-lane PCI Express (PCIe x4) host interface
- Five level memory structure (8.5 GB+).  
Maximum sustain throughput of **3,259 GB/s** for internal memories and **10 GB/s** for DRAMs as follows:
  - ✓ Up to 1040 M9K (9K-bit) DPRAM blocks (1.15MB with **3,000 GB/s** throughput @ 300Mhz)
  - ✓ Up to 48 M144K (144K-bit) RAM blocks (0.85MB with **259 GB/s** throughput @ 300Mhz)
  - ✓ Up to 6,750 MLAB (320-bit) RAM blocks
  - ✓ A 512 MB DDR2 memory with **4 GB/s** sustain throughput using up to 8 ports. (Up to 16 ports with lower access rate)
  - ✓ 2 DDR2 SODIMMs with up to **4 GB** each at a maximum sustain throughput of **6 GB/s** (designed to support future 8GB SODIMMS)
  - ✓ Onboard SRAM options on SODIMM modules
- Supports 2 PROCe III Daughter Boards:  
Camera Links, User's Ethernet and other interfaces
- Typical system frequencies: 100-325 MHz.
- Flexible clocking system.
- Volatile and non volatile design security
- Supported by GiDEL's **PROC Developer's Kits**

### Benefits

- Leading edge performance
- Advance development tools
- Low power consumption
- Maintainability
- Reliability
- Long life cycle



### Overview

The **PROCe III™** system provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory resulting in a powerful and highly flexible system. The **PROCe III** can be hosted via 4-lane PCI Express. The performance, memory and add-on daughter boards' flexible architecture enable the system to meet almost any computation needs. In addition to 512MB on-board memory, two SODIMM sockets provide up to 8GB of memory or additional connectivity and logic. Abundant memory conjoined with fast PCIe connection enable strong co-processing between a standard PC operating system and the FPGA acceleration. The **PROCe III** system, with GiDEL's **PROC Developer's Kit** and tools, offers an incredible performance yet supports quick implementation of your unique design. It is done by eliminating the need for a high-speed board design, a PCI Express application driver, board constraints and environment FPGA code. The generated HDL code enables high throughput, easy-to-use parallel access to large memories. As a result, designers can focus on their proprietary value-added design. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them.

## Development Environment

The **PROCDeveloper's Kit**, GiDEL's intuitive design and debug environment, facilitates design development effort on the **PROCe III** system. The kit contains **PROCWizard™**, **PROCMultiPort™** IPs, **Quartus** and **USBBlaster**, and a **PROCHIL™** option.

The **PROCWizard** performs hardware initialization and automatically generates the following:

- Interface documentation in HTML or Microsoft Word.
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the PROC board.
- Top-level designs, interface modules / entities and on-board memory controllers for the application use.
- Device constraints (as pin-outs).

The **PROCMultiPort** core IP provides simple access as FIFOs and frame delays to the on-board DRAM. It enables parallel access to the on-board memory while enabling to split the physical memory into multiple logical memories.

As a result the main benefits are:

- Simplifies design and enhances system performance.
- Replaces the need for inventory of special memories by using standard memory and IP.

The **USBBlaster** enables visibility of internal signals using the available FPGA memory.

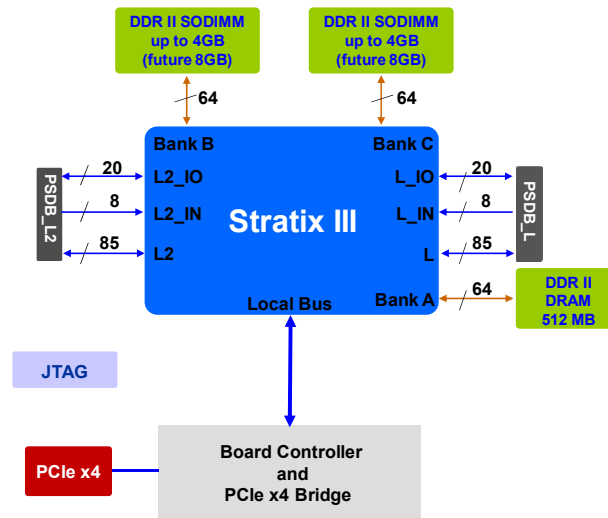
## PROCCessing Performance examples

Algorithm	Data flow rate	% critical resource of Stratix III logic		
		80E	110E	150L
1024*1024 FFT Width 12 bit Transform time 5.7mS	370 MHz	11%	8.2%	10%
9*9 filter symmetric 12 bit data 16 bit coefficients	336 MB/s	1%	<1%	<1%
7*7 8bit Median filter	255 MHz	11%	8.4%	6.3%
Circle open / close with radius up to 15 pixels 8 bit per pixel	323 MHz	5%	3.8%	2.9%
Threshold, add, subtract, 10→ 8 LUT,	>> 640 MHz	<< 1%	<< 1%	<< 1%

\* Due to the different resource usage, better utilization is expected in a full design.

\* For faster operation, use a multi-channel design.

\* For 260 and 340L performance data, contact GiDEL.



**PROCe III board diagram**



[www.gidel.com](http://www.gidel.com)

**Worldwide:**  
2 Ha'ilan Street, P.O. Box 281  
Or Akiva, 30600, Israel  
Tel: +972 - 4610 - 2500  
Fax: +972 - 4610 - 2501  
Email: [sales\\_eu@gidel.com](mailto:sales_eu@gidel.com)

**USA:**  
1600 Wyatt Drive Suite 1  
Santa Clara, CA 95054, USA  
Tel: 1 - 408 - 969 - 0389  
Fax: 1 - 866 - 615 - 6810  
Email: [sales\\_usa@gidel.com](mailto:sales_usa@gidel.com)