

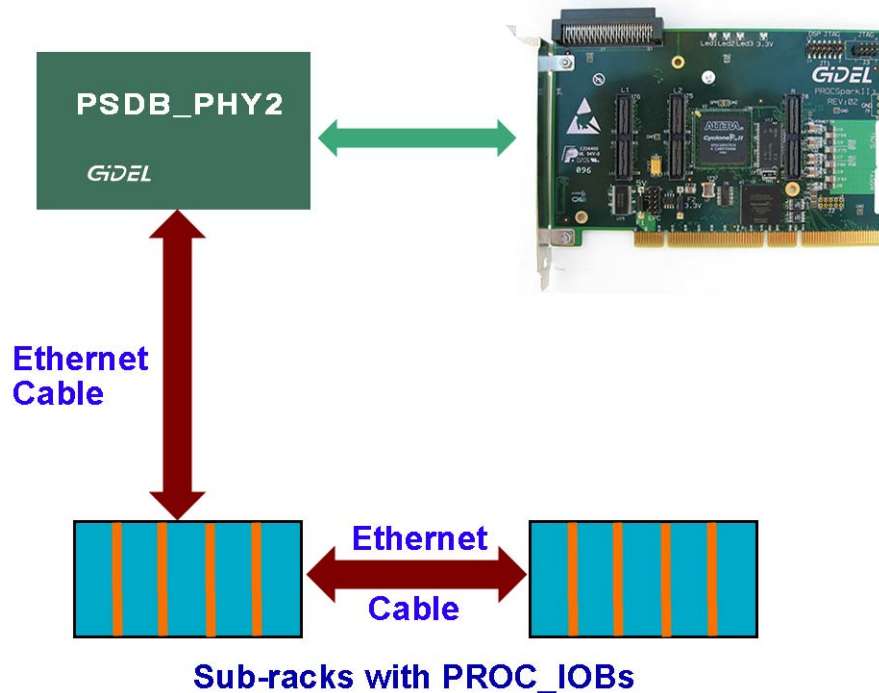
PROC_IO™ System

Overview

The IO System is designed to enable a scalable system to have a huge amount of I/Os with real-time control by central FPGA(s) and host SW.

The system has three main parts: The IO_Rack/IOB, PSDB_IO and the PROC Board connected via cable.

- A half-size 19" IO_Rack system containing 5 IOBs
- A full-size 19" IO_Rack system containing 10 IOBs
- A single board stand-alone IOB system



Main Features

The IO_Rack will contain 1 to 6 IOBs.

IOB Key features:

- 64 Input channels TTL level
- 32 Output channels TTL level (Darlington driver)
- 8 channel A/D converter with minimum 12-bit resolution ($\pm 10V$ input).
- 8 channel D/A converter with minimum 12-bit resolution ($\pm 10V$ output).
- I²C serial interface (physical level).
- The bandwidth for each I/O pin is 500Hz.
- Operating Status LED + two user LEDs.
- Optional to drive the output channels via external PS higher than TTL level (in groups)
- Optional Pull up Pull down for I/O digital channels - in groups, exact spec TBD.
- Security code: a unique code for each customer to enable product protection.

Communications:

- The IOB I/O pins, ADC, DAC and I2C are controlled from the PROC Board FPGA. Each I/O can communicate in one of two ways:
 - Directly in the FPGA - by having a dedicated signal in the FPGA to update the output pin, or a signal in the FPGA with the input pin logic.
 - Via software - write to the output pins or read from the input pins by accessing to specified memory locations. User may also use structure in order to access individual field (any # of I/Os from 1 to 31 in a DWORD boundary).
- Communication from PROC Board via the PSDB_IO and the IO_Racks will be made by serial interface implemented in the FPGA using up to 20 meters of a twisted pair cable with (exact cable & connectors TBD).
- Electric connection between PSDB_IO and IO_Rack: TBD (RS422 or Opto-Couplers).
- Optional for operating the IOB without the IO_Rack (single I/O board) by connecting the IOB to the PROCS Board directly via the PSDB_IO with a twisted pair cable (same as for the IO_Rack), and external power supply provided by the user.
- Communication between the IO_Racks will be via flat cable.
- The output interface from each I/O board will be via standard rugged cable (type of cable & connectors TBD).
- The FPGA algorithm will be loaded from the file via the PCI bus.



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