

A success experience with GiDEL's PROCSuperStar

Research group	Rensselaer VLSI System Architecture Laboratory, Rensselaer Polytechnic Institute, Troy, NY
Design Challenge	Develop a real-time low-density parity-check (LDPC) code decoding simulator to investigate the potential of LDPC code in real-life applications demanding very low error rate
Results	Implemented a real-time simulator with the average decoding throughput of 1Gbps using Gidel's PROCSuperStar

Because of their excellent error-correcting performance and highly parallel decoding scheme, low-density parity-check (LDPC) codes have become a topic of great current interest, e.g., LDPC codes have been recently adopted by the digital video broadcasting (DVB) and are being seriously considered by IEEE 802 standard committees on 10G Ethernet, wireless local area network, and wireless metropolitan area network. LDPC codes also hold great promise for being used in next-generation magnetic storage and holographic storage.

However, accurate evaluation of the LDPC error-correcting performance heavily depends on extensive Monte Carlo

simulation. As a result, for applications targeting very low error rate, it will require paramount computing power. For example, to evaluate the performance of LDPC codes for IEEE 10G Ethernet standardization, in 2004, researchers at Japan employed the AIST (National Institute of Advanced Industrial Science and Technology) Super Cluster consisting of **256** 3GHz processors to simulate **2×10^{13}** bits in **two weeks**. Clearly, the demand for such high computing power makes it very difficult to effectively investigate and compare the performance of various LDPC code construction schemes and overall error-correcting system design. In this regard, a high-speed LDPC decoding hardware simulator is necessary.

Based on GiDEL's PROCSuperStar platform that contains three Altera Stratix 80 devices, the researchers at Rensselaer VLSI System Architecture Laboratory successfully implemented a real-time LDPC decoding simulator that can achieve an average decoding throughput of 1Gbps when targeting on the frame error rate less than 10^{-6} . It provides the capability of simulating 8×10^{13} bits within **only one day**. This is fastest LDPC decoding simulator ever reported in the open resource. The excellent system performance, the abundant inter-chip interconnection, and user-friendly design software of the GiDEL's PROCSuperStar play a key role in the successful implementation of this record-breaking real-time LDPC decoding simulator.