

**ESNUG**

( ESNUG 486 Item 6 ) ----- [07/30/10]

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Subject: User review of Gidel ProcStar II and a first look at ProcSoC 3

Hi, John,

I have used Gidel's ProcStar ASIC prototyping product since 2004, then moved to their ProcStar II in 2006. This is my production experience with their 4 Altera Stratix II 180 FPGA hardware, and its associated development kit.

In addition, I've added my evaluation of Gidel's newest ProcSoC 3, which has between 2-6 Stratix IV 820 FPGAs (we evaluated the version with 2 FPGAs).

We have a 4 M+ gate design to fit into ProcSTAR and 8 M+ design we will use for ProcSoC. The designs will run from 100 MHz to 600 MHz.

**ProcStar II**

We mainly used ProcStar II for SOC prototyping. We ran all 4 FPGAs in ProcStar II at the same time with the following speeds:

- Between FPGAs: 50 MHz
- Inside the FPGAs: 100 MHz

We manually partitioned our design by function. We switched to a simpler bus structure to fit our interconnect into the FPGA board design. Gidel provides good quality global clock with minimum skew so we have never had a problem with synchronization among its different FPGAs.

As long as the design can fit into FPGA, our design size does not impact the speed. The size is mainly decided by Altera FPGA type. The Stratix II 180-4A has 717,600 Logic Elements (LE). According to Gidel, this typically supports 2.5 to 6.5 million gates, because a typical ASIC design uses 3.5 to 9 logic gates per LE and a typical FPGA design uses 10 to 20 ASIC gates per LE. For faster designs using more flip-flops, the gates-per-LE will be high and for low power design using more logic between flip-flops the gates-per-LE will be lower.

We can run ProcStar either in standalone mode or plugged into a PC. We fed specific test data to correlate with our simulation environment through ProcStar's MegaFIFO IP for hardware debugging. It was easy to configure the on-board clock speed. We also used Gidel's ProcMultiPort memory model IP, mostly to store our test vector data.

ProcStar helped us catch multiple design problems, in particular:

- Stress testing. We could run complex testing scenarios for a long time.
- Software/hardware interface issues.

ProcStar's Limitations:

1. There's a limited number of interconnects between FPGA. This issue was addressed with ProcSoC.
2. In standalone mode, it does not come with a power supply or a power connector that is easy to hook up. ProcSoC has both.
3. The fan attached to the Altera FPGAs sometimes stopped working and sometimes created quite some noise. However, Gidel responded to our support request within 8 hours. Also, they appear to have remedied this issue in ProcSoC 3 by redesigning it to use heat sinks instead of a fan, plus they have mounted an additional fan on the ProcSoC chassis.

**ProcSoC 3**

We starting evaluated Gidel's newer ProcSoC in-house in May 2010 and decided to purchase it in June. From an ASIC prototyping point of view, ProcSoC 3 includes all of the ProcStar II functionality (including the software and IP), plus it has more interconnect capability and flexibility.

Our key evaluation criteria for ProcSoC 3 was:

1. More FPGA Interconnections. ProcSoC 3 provides more connections between two FPGAs. When we used ProcStar II, we needed to convert our interface protocol to a simpler one with fewer pin counts, and this created a discrepancy. For ProcSoC 3, we can keep the same design as our ASIC without making any modifications, which we prefer from verification point of view.
2. Simplicity of use. When I want to change the interconnect, I only need to rearrange the cables. This means I don't need to go through

configurations and wonder if it will work or not. The I/O connectors are all lined up on the front and back, it's easy to make all the connections.

3. Robustness. ProcSoC 3 is a standalone box which has a more solid design than ProcStar II, including having its own casing, cooling, Ethernet, and power supply. The ProcSoC 3 board is isolated in the box so our engineers do not need to touch it directly, reducing the chance that they will break it.

#### Expected Speed and Capacity

From our eval ProcStar II, we are EXPECTING 133 MHz for an ARM 11 core processor on the ProcSoC 3 Altera Stratix IV 820. We have NOT YET verified ProcSoC 3's capacity limits, but according to Gidel:

- Each 'Procl2M' module has two Stratix IV 820E FPGAs, and each Stratix IV 820E has 813,050 LEs.
- In most cases the FPGAs have much more embedded memory capacity than required so ProcSoC 3's capacity is based on the pure logic capacity.
- For pure ASIC prototyping, one ProcSoC 3 can have 1 to 3 Procl2M modules, so its capacity ranges from 5.7 to 44 M gates.
- One ProcSoC 10 can have from 2 to 10 Procl2M modules, so its capacity ranges from 11.4 to 146 M gates.
- Three ProcSoC 10 full capacity systems cascaded together will have a capacity range from 170 to 439 M gates.

(Again, this is what Gidel TELLS us; we haven't confirmed this!)

Our ASIC SoC designs have many connections between design blocks so it is important for us to have interconnect flexibility. In this regard, ProcSoC 3 is very flexible -- we can make direct connections between the FPGAs. We can fit in a new design in very easily. All we have to do is to rearrange the cables.

ProcSoC 3 is very portable and the power supply is built in. The size of the box is fairly compact. The dimensions are: height - 150 mm/5.90 inch, width - 315 mm/12.40 inch, and depth - 235 mm/9.25 inch. It is easy to manage through any PC system from desktop to notebook through Ethernet. When we travel with it, all we need to do is to connect a notebook computer to it; we do not need a desktop or a huge power supply. So we can actually carry it with us to travel to other countries and work with other groups.

ProcStar II has already saved us respins - our recent production chip worked the first time we went to silicon. Plus Gidel always shipped products on time, and they provide good design examples and documentation. We're assuming that their newer ProcSoC 3 will be as good, if not better.

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