

GiDEL Announces The Availability Of TotalHistory™

A New Level in ASIC Prototyping and FPGA Debug

June 14, 2010, Anaheim, CA – GiDEL Inc., the first company to provide ASIC Prototyping Systems announced today the availability of TotalHistory™, the most advanced debugging feature available in today's ASIC Prototyping solutions and FPGA based systems.

TotalHistory is a software only solution enabling users to define a list of signals in the design which they want to trace at full system speed. There is practically no limit on the number of signals traced. The user can then view the trace using a waveform viewer to debug and validate the design. Optionally, an API is available for queries by advanced users.

“TotalHistory enables users to have visibility of any signal in their designs, for virtually unlimited trace depth, with no or minimal degradation in performance”, said Reuven Wientraub, GiDEL's Founder and CTO. “TotalHistory opens the horizon for new debug and validation methodologies including dumping internal data while running at customer site, finding random glitches in long runs, etc. It leverages the unique architecture of our systems eliminating the need of additional costly hardware.”

TotalHistory is available with GiDEL's PROC_SoC ASIC Prototyping Systems and PROC Boards FPGA-based High Performance Computing (HPC) accelerators.

GiDEL is demonstrating TotalHistory at this year's Design Automation Conference in Anaheim, California on June 14-16, at booth 912.

For more information on GiDEL's PROC_SoC ASIC Prototyping Systems please see www.gidel.com/asic-prototyping.

About GiDEL

GiDEL is the first company to introduce ASIC Prototyping Systems and FPGA-based Vision, imaging and HPC acceleration solutions. It consistently leads the market with cutting-edge architectures, solutions and methodologies.

For more information please see www.gidel.com

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